Choonki Jang

Curriculum Vitae

School of Computer Science and Engineering,
Seoul National University,
Seoul 151-744, Korea
✉ *choonki@aces.snu.ac.kr*
http://aces.snu.ac.kr/~choonki

Education

Mar. 2004 - present **Ph.D. student in Computer Science and Engineering**,
Seoul National University, Seoul, Korea.
Advisor: Jaejin Lee

Mar. 1998 - Feb. 2003 **B.S. student in Computer Science and Engineering**,
Seoul National University, Seoul, Korea.

Research Interests

Compilers, post-pass optimization, programming languages, runtime systems for multi-cores/manycores, and embedded systems

Experience

Mar. 2008 - Jun. 2008 **Part-time Lecturer**,
School of Electrical and Computer Science, City University of Seoul, Seoul, Korea.
Compilers

Jul. 2007 - Aug. 2007 **Summer Intern**,
Samsung Advanced Institute of Technology, Kyoungki, Korea.
Memory hierarchy optimization for Reconfigurable Processor

Honors and Awards

Jun. 2011 **Third place**,
ICS '11 ACM Student Research Competition.
An Automatic Code Overlaying Technique for Multicores with Explicitly-Managed Memory Hierarchies

Feb. 2010 **Gold Prize**,
16th SAMSUNG HumanTech Thesis Competition, Korea.
Automatic Code Overlay Generation and Partially Redundant Code Fetch Elimination

Projects

Jun. 2008 - Feb. 2010 **Memory Optimization Technique for Coarse-Grained Reconfigurable Processors**,
Samsung Eletronics, Korea.

- Data placement technique for multi-core architectures
- Data placement technique to reduce bank conflicts for multi-banked memory
- Data overlay technique to reduce the memory footprints due to data accesses

Dec. 2006 - Nov. 2007 **Memory Hierarchy Management for Reconfigurable Processors**,
Samsung Eletronics, Korea.

- Development of cycle-accurate CGRA architecture simulator in SoC Designer
- Instruction-scheduling-aware data partitioning technique

Mar. 2005 - Feb. 2007 **Embedded S/W Design and Verification Techniques for MPSoC**, *Ministry of Information and Communication*, Korea.

- Design and Implementation of multi-core architecture simulator

Mar. 2004 - Feb. 2007 **Low Power and High Performance Embedded Video Processors**, *Ministry of Information and Communication*, Korea.

- VLIW instruction scheduling at postpass
- Porting GCC for embedded VLIW processor

Publications

[1] Choonki Jang, Jun Lee, Sangmin Seo, and Jaejin Lee. An Automatic Code Overlaying Technique for Multicores with Explicitly-Managed Memory Hierarchies. In *Proceedings of the 2012 International Symposium on Code Generation and Optimization*, CGO '12, pages —, 2012.

[2] Seungkyun Kim, Kiwon Kwon, Chihun Kim, Choonki Jang, Jaejin Lee, and Sang Lyul Min. Demand paging techniques for flash memory using compiler post-pass optimizations. *ACM Transations on Embedded Computing System*, 10:40:1–40:29, November 2011.

[3] Choonki Jang. SRC: An Automatic Code Overlaying Technique for Multicores with Explicitly-Managed Memory Hierarchies. In *Proceedings of the International Conference on Supercomputing*, Student research competition poster presentation in ICS '11, pages 377–377, 2011.

[4] Choonki Jang, Jungwon Kim, Jaejin Lee, Hee-Seok Kim, Dong-Hoon Yoo, Sukjin Kim, Hong-Seok Kim, and Soojung Ryu. An Instruction-Scheduling-Aware Data Partitioning Technique for Coarse-Grained Reconfigurable Architectures. In *Proceedings of the 2011 ACM SIGPLAN-SIGBED conference on Languages, compilers, and tools for embedded systems*, LCTES '11, pages 151–160, 2011. (17/51, 33.3%).

[5] Bernhard Egger, Seungkyun Kim, Choonki Jang, Jaejin Lee, Sang Lyul Min, and Heonshik Shin. Scratchpad Memory Management Techniques for Code in Embedded Systems without an MMU. *IEEE Transactions on Computer*, 59:1047–1062, August 2010.

[6] Jaejin Lee, Junghyun Kim, Choonki Jang, Seungkyun Kim, Bernhard Egger, Kwangsub Kim, and SangYong Han. FaCSim: a fast and cycle-accurate architecture simulator for embedded systems. In *Proceedings of the 2008 ACM SIGPLAN-SIGBED conference on Languages, compilers, and tools for embedded systems*, LCTES '08, pages 89–100, 2008. (17/68, 25.4%).

[7] Bernhard Egger, Chihun Kim, Choonki Jang, Yoonsung Nam, Jaejin Lee, and Sang Lyul Min. A dynamic code placement technique for scratchpad memory using postpass optimization. In *Proceedings of the 2006 international conference on Compilers, architecture and synthesis for embedded systems*, CASES '06, pages 223–233, 2006. (25/100, 25.0%).